Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) In a high data rate receiver for an FSK data transmission system having a data transfer protocol, a digital FSK demodulator for demodulating an FSK signal having a data rate from a carrier signal having a pair of carrier frequencies, the digital FSK demodulator generating a serial data bit stream based on the FSK carrier signal and generating a synchronized constant frequency clock signal from the carrier frequencies based on the data transfer protocol for sampling the serial data bit stream wherein both the data transfer protocol and the demodulator are fully digital to make the system robust.

2. (Original) The demodulator as claimed in claim 1, wherein the data rate is greater than one million bits per second.

3. (Original) The demodulator as claimed in claim 1, wherein the data rate approximates the carrier frequencies.

4. (Original) The demodulator as claimed in claim 1, wherein the carrier frequency is less than about 25 megahertz and more than about 1 megahertz.

5. (Original) The demodulator as claimed in claim 1, wherein one of the carrier frequencies is approximately twice the other carrier frequency so that a duration of each data bit is substantially the same, independent of its value.

6. (Original) The demodulator as claimed in claim 1, wherein the demodulator also detects an error in the FSK carrier signal based on the protocol and provides a corresponding error signal.

7. (Original) The demodulator as claimed in claim 1, wherein the demodulator also digitally measures the period of each received positive half cycle of the FSK

carrier signal to obtain a series of pulses which distinguish between long and short FSK carrier cycles.

8. (Original) The demodulator as claimed in claim 7, wherein the demodulator includes an n-bit counter that runs with a clock time-base, f_{TB}, having a substantially constant frequency at a rate substantially higher than the FSK carrier frequencies, f_1 and f_0, to digitally measure the periods.

9. (Original) The demodulator as claimed in claim 1, wherein the system is a magnetically powered wireless system.

10. (Original) The demodulator as claimed in 9, wherein the receiver is a wireless biomedical implant.

11. (Currently Amended) An FSK demodulator chip for an FSK data transmission system having a fully digital data transfer protocol, the chip comprising:

a substrate; and

a digital <u>FSK</u> demodulator formed on the substrate for demodulating an FSK signal having a data rate from a carrier signal having a pair of carrier frequencies wherein the demodulator generates a serial data bit stream based on the FSK carrier signal and generates a synchronized constant frequency clock signal from the carrier frequencies based on the data transfer protocol for sampling the serial data bit stream and wherein the demodulator is fully digital to minimize the amount of surface area occupied by the demodulator on the substrate.

12. (Original) The chip as claimed in claim 11, wherein the data rate is greater than one million bits per second.

13. (Original) The chip as claimed in claim 11, wherein the data rate approximates the carrier frequencies.

14. (Original) The chip as claimed in claim 11, wherein the carrier frequency is less than about 25 megahertz and more than about 1 megahertz.

15. (Original) The chip as claimed in claim 11, wherein one of the carrier frequencies is approximately twice the other carrier frequency so that a duration of each data bit is substantially the same, independent of its value.

16. (Original) The chip as claimed in claim 11, wherein the demodulator also detects an error in the FSK carrier signal based on the protocol and provides a corresponding error signal.

17. (Original) The chip as claimed in claim 11, wherein the demodulator also digitally measures the period of each received positive half cycle of the FSK carrier signal to obtain a series of pulses which distinguish between long and short FSK carrier cycles.

18. (Original) The chip as claimed in claim 17, wherein the demodulator includes an n-bit counter that runs with a clock time-base f_{TB}, having a substantially constant frequency at a rate substantially higher than the FSK carrier frequencies, f_1 and f_0, to digitally measure the periods.

19. (Original) The chip as claimed in claim 11, wherein the system is a magnetically powered wireless system.

20. (Original) A method for demodulating an FSK signal having a data rate from a carrier signal having a pair of carrier frequencies in an FSK transmission system having a digital data transfer protocol, the method comprising:

digitally measuring the period of each received positive half cycle of the FSK carrier signal to obtain a series of pulses which distinguish between long and short FSK carrier cycles;

digitally generating a serial data bit stream based on the FSK carrier signal and the series of pulses; and

digitally generating a synchronized constant frequency clock signal from the carrier frequencies based on the digital data transfer protocol and the series of pulses.